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SUMMARY

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ARHITECTURI CU INTERFAȚĂ DIGITALĂ DIRECTĂ PENTRU SENZORI DE TIP CMOS HALL

DIRECT-TO-DIGITAL INTERFACES FOR CMOS HALL SENSORS

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Chapter 1

Introduction

Automotive, industrial and consumer applications are complex systems that require sensor solutions to monitor specific parameters, process the acquired information and respond to the environment in real-time. The most general operation principle consists of a sensor IC (Integrated Circuit), a controller unit and an actuator.

The interface between the sensor and the controller may be digital or analog. A digital interface is easier to use and provides a higher degree of immunity to disturbances and noise which may be significant in harsh automotive environments. While an analog output provides a high resolution signal that also captures fast changes in the measured parameter, it's important to note that a digital representation of the signal is anyway required in the controller to facilitate the implementation of complex hardware or software algorithms.

Within the sensor market, next to temperature, pressure and inertial transducers, magnetic sensors play a key role in enabling precise control of advanced systems. While traditionally the automotive market has been responsible for the majority of revenues, the consumer end-market is poised to overtake it in volume, with an estimated of about 7 billion units by 2029 [1], driven by applications such as optical image stabilization (OIS) and eCompass, but also joysticks or virtual reality (VR) headsets.

Magnetic field sensors provide accurate detection of angular, linear and 3D position, as well as rotational movements [2]. Their contactless nature is especially useful in terms of robustness, reliability and durability. There are many magnetic sensing technologies [3], i.e., physical effects that transduce magnetic field into an electrical signal. A few of them are resistive-based, such as anisotropic magnetoresistance (AMR), giant magnetoresistance (GMR) and tunnel magnetoresistance (TMR) effects. These are highly sensitive devices, but their accuracy is limited to $\sim$5% of the full scale range by offset and hysteretic effects.

In contrast to these, the Hall effect is non-resistive. Silicon (Si) Hall effect sensors are generally preferred from a cost perspective, as ICs are typically manufactured in Complementary Metal-Oxide-Semiconductor (CMOS) technology. They offer excellent linearity even in strong magnetic field (in the Tesla range) without showing hysteresis

or saturation effects [4]. This makes them well-suited for modern applications that demand stray field robustness, close magnet spacing and varying airgaps, resulting in requirements of wide magnetic range at the same time with low offset and noise. Even with a Hall plate sensitivity 100x lower than that of a TMR sensor, the accuracy can still exceed 0.1% of the full scale range when the special spinning-current technique is applied.

The typical signal processing path is analog based, consisting of an amplifier, a filter and an output buffer, together with offset reduction techniques such as spinning and chopping. Efforts are made in the direction of less complex and more digital oriented sensor interface systems. Direct-to-digital approaches were used with success for many types of sensors as well as for Hall sensors [5], but progress still remains to be done in terms of magnetic range, area and power consumption.

Modern applications require wider magnetic ranges to accommodate a diverse array of magnets and air-gaps. At the same time, the ability to sense accurately even weak signals remains an important feature, which finally translates into low offset and low noise requirements. Simultaneously, there is a need to include more processing power on chip. This allows for the integration of additional capabilities, such as linearization, gain, and offset correction, which further enhance the overall performance and accuracy of the system [2]. Additionally, challenges in robotics applications such as tactile sensing can be addressed through a multimodal approach, including 3D Hall sensors, but intensive digital signal processing is required. Finally, consumer applications necessitate lower supply voltages, in the range of 1.5 V or even 1.0 V, and low current consumption.

The objective of this doctoral thesis is to prove that direct-to-digital sensor interfaces – connecting the analog-to-digital converter (ADC) directly to the magnetic sensor – are capable of solving all the described challenges simultaneously. Removing the preamplifier enables wider magnetic ranges, as the sensor output voltage, even in the case of Tesla signals, is in the order of tens of millivolts, which can be easily accommodated by an ADC, even in the presence of large initial offsets and low supply voltages. No compromises need to be done in terms of performance: the energy and area previously invested into the preamplifier will be redirected to the input stage of the converter to maintain the same noise levels as before. Particular types of converters, namely continuous-time (CT) feedback-compensated sigma-delta ($\Sigma\Delta$) ADCs, ensure anti-aliasing functionality, avoiding noise degradation from this perspective. The offset rejection techniques from analog interfacing can be adapted and even improved, to allow the same or even better residual offset.

To demonstrate the potential of direct-to-digital interfaces for CMOS Hall sensors, two prototypes were realized in a 130 nm technology, featuring several technical innovations and providing a scalable solution that can be easily adapted to more advanced technology nodes.

Chapter 2

The Hall Device

The Hall effect appears when a conductor or a semiconductor is biased with a constant current I while a magnetic field B is present. The charge carriers that move through the (semi-)conductor experience a Lorentz force and an electrical field is created that balances the charge displacement. The resulting voltage is the Hall voltage (Fig. 2.1a), which has a strong dependence on the applied current, geometry and material properties [6].

For reliable operation in various applications, the Hall sensor's accompanying IC must ensure stable sensitivity over temperature, process, and lifetime variations [4]. This requires low offset, low noise, low temperature and stress cross-sensitivity, and low current consumption, with key device parameters being sensitivity, offset, noise, and resistance.

The Hall resistance R_{Hall} is crucial as it affects thermal noise and current consumption. Absolute sensitivity defines how the magnetic signal is translated into an electrical signal and is measured in V/T. Higher sensitivity improves the signal to noise ratio (SNR) and reduces the impact of readout electronics inaccuracies on the magnetic signal.

For typical bias voltages of 1-2 V and a few mA current consumption, the absolute sensitivity is in the range of 50 to 100 μV/mT [4, 7]. This means that field strengths of 1 mT produce Hall voltage signals in the tens of μV level. The transducer voltage is finally $v_{Hall}\,[V] = S\,[V/T] \cdot B\,[T] + v_{os}[V]$.

Offset (v_{os}), or zero-point error, limits the minimum signal that the transducer may sense. It is defined as the output voltage at 0 mT magnetic field, and it appears mainly due to mechanical stress and processing imperfections [6, 8]. Trimming is not effective because the offset has a strong and non-linear temperature, stress and lifetime dependency.

The offset can be reduced by adequately connecting 2 or 4 Hall plates in parallel [4] in an orthogonal manner to cancel out asymmetries. The limited matching of the devices, especially in the presence of stress, creates the incentive for dynamic cancellation techniques. Ref. [8] proposed to dynamically change the current direction in a single device to cancel processing gradients without requiring matching between multiple

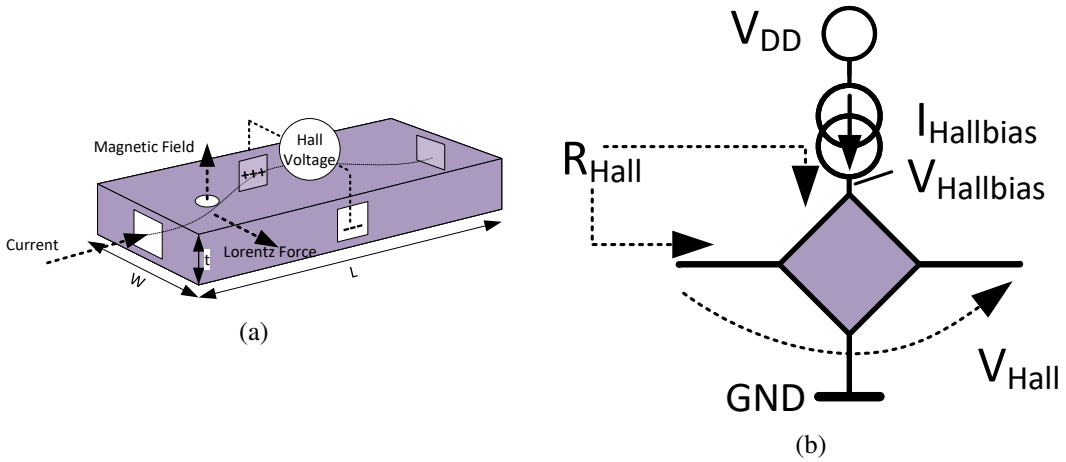


Fig. 2.1 (a) Simplified operation of the Hall effect (b) Simplified diagram of Hall sensor bias.

devices. This approach is known as the spinning-current technique. As long as the offset sources of the single Hall plate remain constant during current rotation, the offset can be completely eliminated through averaging or filtering.

In an actual implementation, the current direction is made to spin by one MOS multiplexer, while the sense terminals are connected to the readout stage by another one. By interchanging the output terminals during the 90°and 270°phases [9], the offset of the amplifier can be processed together with the Hall offset (at DC), while the signal is modulated at the F_{chop} frequency. A demodulator is then needed after the amplifier to bring back the signal to baseband.

Temperature and stress gradients, combined with the voltage dependency of the active Hall layer thickness, introduce offset components at that are indistinct from the signal in a 2-phase spinning scheme. This can be generalized to a 4-phase scheme, which allows to distinguish also these secondary effects.

The offset present before the spinning-current technique is applied is called *initial offset*. Even after orthogonal coupling, it may be in the order of 5 to 10 mTrms. The 2nd order initial offsets may account for up to 0.5 mTrms. The modulated offset that needs to be averaged or filtered out is called *offset ripple* and, unless properly rejected, it will contribute to the noise budget.

The remaining offset error that cannot normally be distinguished from the signal, thus finally limiting the system resolution, is called *residual offset* and it stems from contributions that rotate with the current, spatial effects that fold down to DC or dynamic effects like charge injection and clock feedthrough. Standard deviation in the order of tens of μT is considered state-of-the-art [5].

Finally, a note related to the drawback of the dynamic offset cancellation technique. The offset ripple needs to be suppressed by a filter, which reduces the bandwidth and introduces delay. Increasing F_{chop} reduces the offset ripple energy through increased filter attenuation, but it has the drawback of increased spike energy that demodulates into residual offset.

Chapter 3

Readout Circuits for Magnetic Sensors

The Hall signal, typically in the range of microvolts (μV), can be easily overwhelmed by millitesla (mT) level offsets stemming from the sensor itself. Specialized readout circuits, located at the front-end of the signal processing path, condition the signal and must be optimized for noise and offset, often using techniques like chopping. In this thesis, "readout circuits" and "sensor interface" are used interchangeably.

In the case of an IC with analog sensor interface (Fig. 3.1a), the amplifier is noise and offset optimized, while the subsequent stages, such as a filter or an ADC, have more relaxed specifications. A buffer is sometimes used after the filter to provide a low-ohmic output, such that the ADC implementation is agnostic. For certain applications the ADC is placed off-chip and the buffer serves as the final stage of the ASIC (output buffer), but numerous magnetic sensors prefer on-chip ADCs for a robust digital output interface [5, 10–12].

The ADC can be connected directly to the sensor, in what we call a direct-to-digital interface (Fig. 3.1b). The noise requirements of the preamplifier are transferred to the ADC. As there is no explicit anti-alias filter, the ADC must be a continuous-time (CT) sigma-delta ($\Sigma\Delta$) ADC, which inherently provides anti-aliasing functionality [13]. To avoid disturbing the sensor, Gm-C techniques are utilized.

This approach improves dynamic range by avoiding amplifier gain limitations at low supply voltages. Typical sensor outputs are limited to tens of mV, posing no saturation risk in the ADC. Moreover, the direct-to-digital method saves area and power by eliminating preamplifiers, analog filters, buffers and analog offset ripple loops, making it particularly beneficial in advanced technology nodes.

In CMOS technologies, the offset voltage of the readout stage is typically in the millivolt range, limiting sensor accuracy. Trimming is ineffective due to drift, so techniques like auto-zero and chopping are used to reduce offset [14]. However, auto-zero can introduce baseband noise [15], making chopping a preferred choice, especially for continuous-time applications.

The chopping principle, illustrated in Fig. 3.2, modulates the signal with a square wave, separating it from amplifier offset and low frequency noise. After the amplifier, a

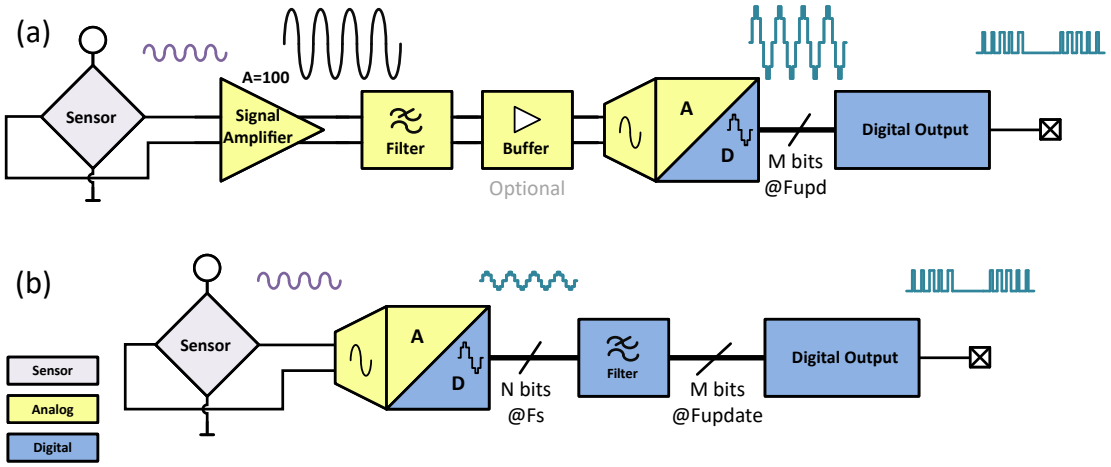


Fig. 3.1 Sensor IC with a) analog b) direct-to-digital sensor interface (readout circuit).

demodulation or "unchopping" stage, returns the signal to baseband, while modulating the offset and 1/f noise to F_{chop}, where they can be filtered out. Setting the filter's cutoff frequency too low would compromise bandwidth and increase area and delay. As an option, analog notch functionality can suppress the offset ripple through sampling, but this introduces noise aliasing [16].

Offset ripple loops offer an alternative [10, 17]. By using an integrator to accumulate the offset and produce a feedback compensation signal which attenuates the ripple in the main path, they allow for a simpler broadband filter with lower delay. This architecture proved to be the most efficient and will be included in multiple variations in the final comparison table.

Analog interfacing has several drawbacks. The numerous analog blocks restrict scaling to lower technology nodes, while increasing dynamic range is difficult due to amplifier gain limitations, which can make subsequent stage errors dominant. Direct-to-digital interfaces can address these challenges.

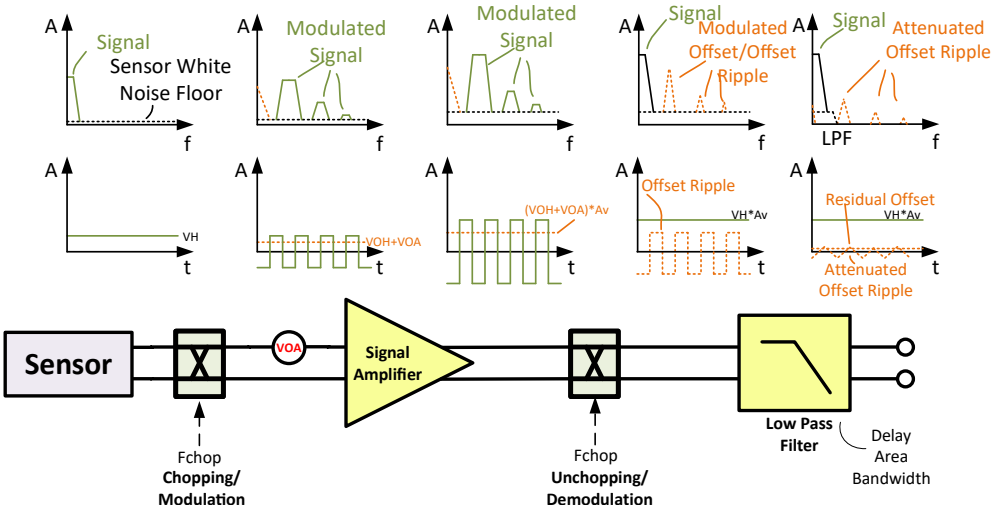


Fig. 3.2 The chopping principle.

Chapter 4

Tracking-based CT-ΣΔ-ADC magnetic sensor with digital offset ripple loops (D2D MS1)

4.1 Introduction

This chapter presents a direct-to-digital architecture with CT-ΣΔ-ADC for a magnetic switching sensor (D2D MS1 = Direct-to-Digital Magnetic Sensor 1). Compared to previous designs, the preamplifier and offset DAC have been eliminated. The magnetic data is accessible at a high resolution and sampling rate prior to the digital comparator, making the signal path suitable for alternative applications such as linear Hall, angle, and current sensing, as long as the bandwidth requirements are limited to tens of kHz. To reduce area, a tracking implementation of the inner loop quantizer is preferred, while digital offset ripple loops are used to suppress the offset in the main path. Together with a custom nano-timing scheme, these techniques result in lower offset and noise density compared to most existing solutions, while also reducing area and power consumption. Primarily due to the enhanced dynamic range, it achieves best FOM in CMOS Hall magnetic sensors, surpassing state of the art by at least 3.1x. This system was presented in our paper [18].

The proposed system (D2D MS1) is shown in Figure 4.1. A Hall sensor, together with its switchbox, outputs a modulated magnetic signal at F_{chop} = 79 kHz. A chopped continuous-time ΣΔ ADC with tracking quantizer and with built-in digital offset ripple loops brings the signal back to baseband, digitizes it and rejects most of the undesired offset components. Any residual F_{chop} artifacts due to the limited resolution of the feedback loops are rejected by a digital notch operated at F_s. An infinite impulse response (IIR) filter sets the final bandwidth of the system to F_{BW} = 14 kHz according to noise requirements. At this point the absolute magnetic information is available at high rate (F_s = 10 MHz) and high resolution (16 bits). It means that the system may

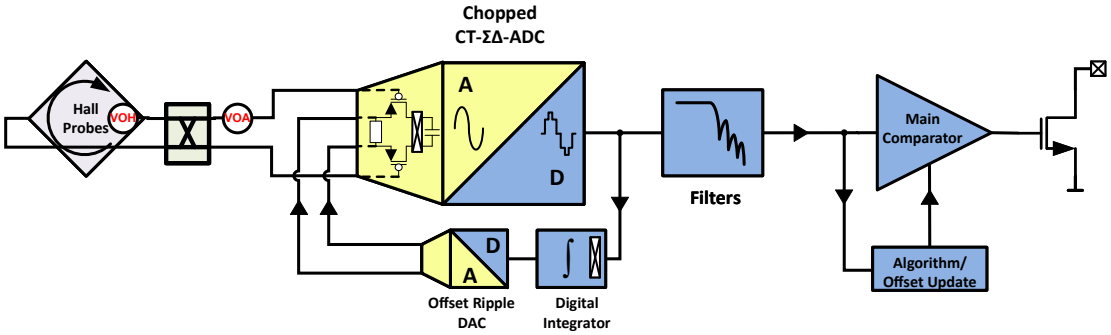


Fig. 4.1 The proposed switching magnetic sensor with direct-to-digital readout interface (D2D MS1).

be used also for any type of linear output sensor. For a switching sensor, a digital comparator must be added on top to drive the output switch. Here, noise in the signal path is converted into time-domain jitter, which is directly proportional to the slope of the input magnetic field. The thresholds are calculated using algorithms that identify the minima and maxima of the signal, typically setting them to 70% of the amplitude with a small, hidden hysteresis.

4.2 Circuit Implementation

The circuit implementation of the main component blocks of the D2D MS1 is described in the following subsections.

4.2.1 Spinning Current Hall Sensor

The spinning current Hall sensor is shown in Figure 4.2. Four Hall plates take 1 mA from a 2.4 V supply. They are placed in parallel, but orthogonally coupled, to reject any local asymmetries. They contribute a 5 nV/$\sqrt{\text{Hz}}$ noise spectral density.

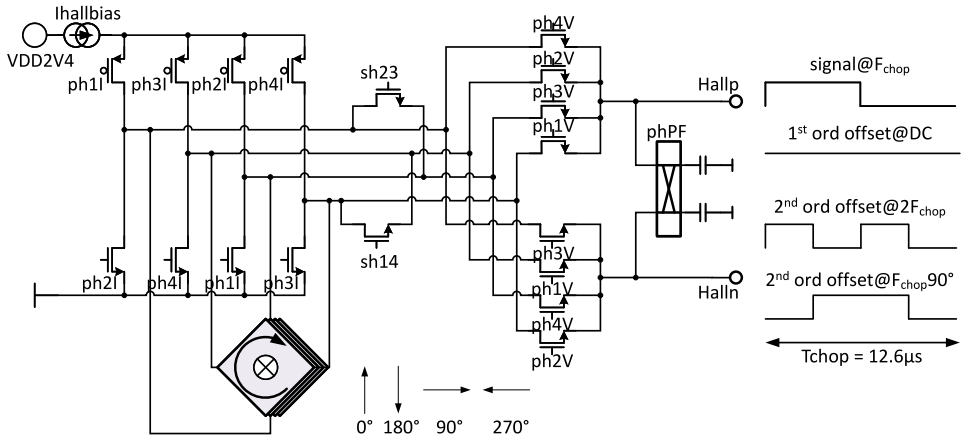


Fig. 4.2 The switchbox used for the spinning current Hall sensor.

A 4-phase spinning scheme is employed to be able to reject also 2nd order effects. The rotation sequence is 0°/180°/90°/270°. This ensures that the signal is modulated at F_{chop}, while the main Hall offset remains at DC. Second order effects are also modulated at $2 \cdot F_{chop}$ and F_{chop} shifted by 90°, where they can still be distinguished from the signal.

In the proposed spinning scheme, two switches (*sh23* and *sh14*) are used to speed up the settling at 90° rotations. They are only activated for a short time. To reduce the effect of the spikes in the presence of mismatches, chopped capacitances are added to the system, driven by the *phPF* clocks.

4.2.2 ADC Implementation

A feedback compensated CT ΣΔ ADC (Fig. 4.3) is chosen to benefit from inherent anti-aliasing functionality [13]. To reduce design complexity, a 1st order loop filter is used, consisting of an integrator, a 6-bit quantizer and 6-bit current steering DAC that implements the modulator's feedback path. The architecture employs chopping to separate the readout stage offset, while digital offset ripple loops are used to suppress it before it reaches the quantizer. The ripple loops reuse the main ΣΔ DAC for their 6 MSBs and require an additional, but not critical, 4-bit DAC to achieve a total 10-bit resolution. Any residual ripple is rejected by a notch and an IIR filter sets the final bandwidth.

The integrator is implemented as a folded cascode with source degeneration followed by capacitors referred to differential virtual ground that also provide common mode stability (Fig. 4.4). For low current consumption, the input stage relies on ΣΔ feedback to linearize its Gm, and thus has an equivalent transconductance strictly inversely proportional to R_{sense}. This makes possible a process stable ADC reference with a

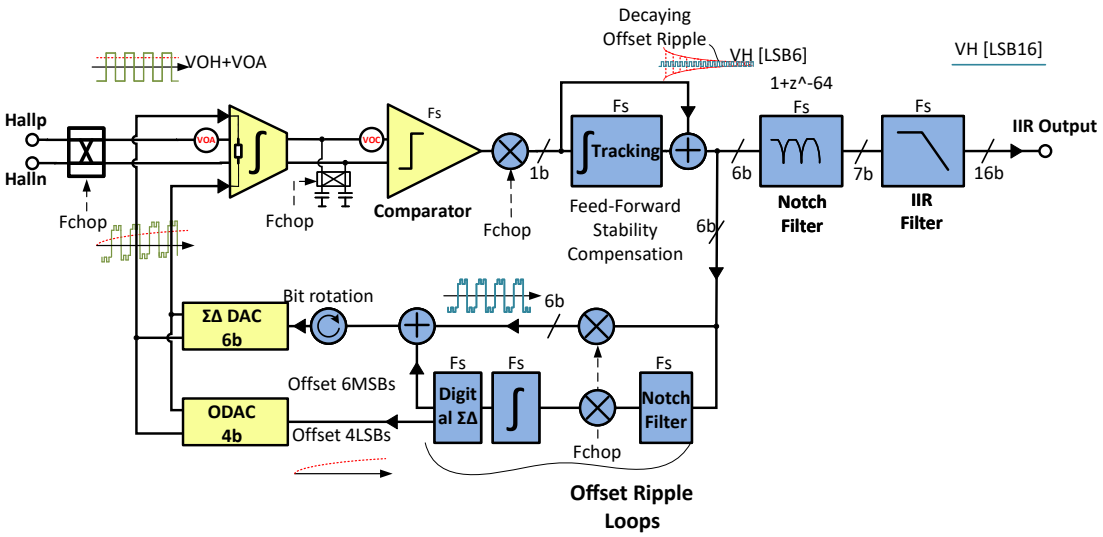


Fig. 4.3 Block diagram of the ADC including the offset ripple loops.

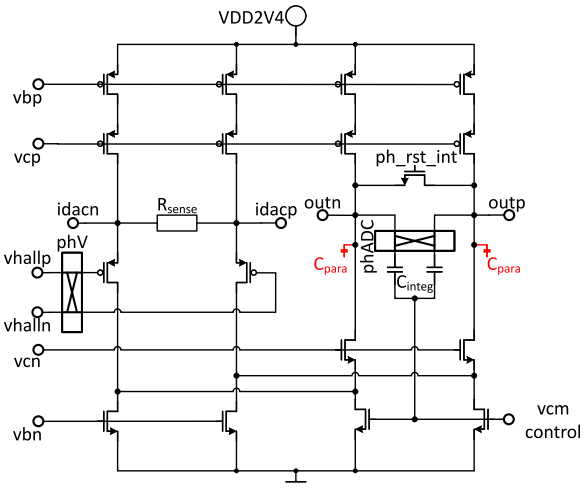


Fig. 4.4 Simplified schematic of the analog integrator.

well-defined temperature coefficient [10], since the DAC current is generated from a bandgap voltage applied to a closely matched resistor.

To make quantization noise negligible, the high oversampling ratio of $F_s/F_{BW}/2 = 357$ is upheld by a 6-bit tracking quantizer which consists of one analog comparator and a digital counter. This is area effective, but it has two disadvantages: it adds a 90° phase shift in the loop thus necessitating feed-forward stability compensation, which is fortunately trivial to implement in the digital domain [5]; and it slews for fast changing input signals. For this reason, the integrating capacitors are chopped to keep the signal in the baseband, while the three feedback loops reduce the offset ripple content.

The 6-bit current-steering DAC is chopped and thermometrically coded in the digital domain. Its output current is injected into the sense resistor. A bit rotation algorithm modulates the DAC non-linear effects around the chopping frequency where they are removed by the main path notch filter.

4.2.3 Timing Sequences

As shown in Fig. 4.5 the 4 spinning phases take 31, 32, 31, 32 clocks respectively [19]. At transitions between two spinning cycles, the following sequence occurs. The measure switches are turned off for 27 ns, but the magnetic signal is still available at the input of the readout stage on the so-called peak filter capacitors that smooth out differential spikes and ensure that the input common mode remains stable. Next, the Hall current is rotated by disabling and enabling the respective current switches *phI* (Fig. 4.2) with a non-overlapping time of 3 ns. The sensor terminals that will drive the readout stage are shorted for 9 ns to quickly discharge their corresponding parasitic capacitors, thus enabling high spinning frequencies. This action is mostly required during 90° transitions, when these nodes need to converge to mid-supply coming either from ground or full supply level [9]. Next, the integrating capacitors are disconnected for 7 ns. In this time

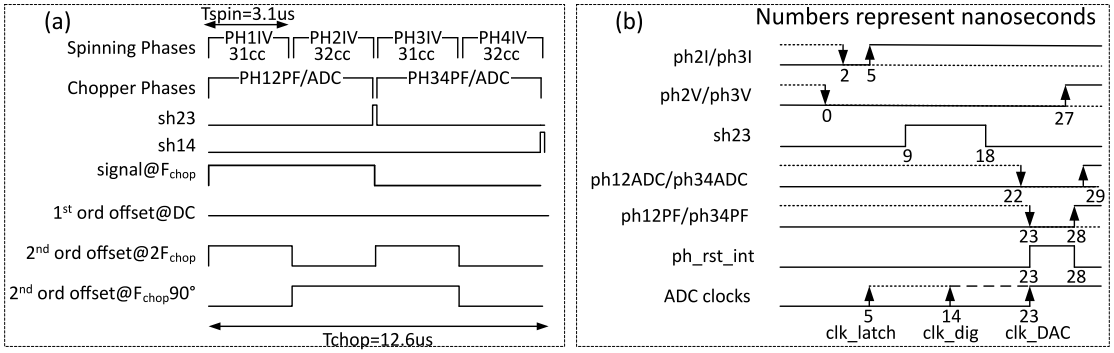


Fig. 4.5 Macro- and nano- timing sequences including detail about the integrator, comparator and DAC.

the peak filter capacitors are reverted, and the output of the gain stage is shorted to release any parasitic charge. The measure switches are then activated, followed by the integrating capacitors.

In a tracking system, there are only two possible future DAC values: the current state incremented or decremented by 1. The digital pre-computes and feeds both options into a multiplexer, allowing the comparator decision to make a rapid selection between them. The delay between the latch in of the integrator output and the injection of the DAC current into the sense resistor accounts for an excess loop delay of 17 ns.

4.2.4 Digital Feedback Offset Ripple Loops Implementation

In a 4-phase system, besides the signal, there are 3 distinguishable offset ripple parts [17]. In the current design, after the proper demodulation, three digital integrator circuits are used to slowly accumulate each of these components, which then decay in the tracking path (Fig. 4.6). Their contributions are summed in a 17-bit register. To reduce area, the main ΣΔ DAC carries also the first 6 MSBs of the offset information. An additional DAC, that only needs to be monotonic, takes the subsequent 4 bits increasing the resolution of the ripple rejection loop to 10 bits. Finally, the remainder of 7 bits are fed back in a digital ΣΔ configuration to at least avoid propagating any truncation errors. The side paths are operated at F_s, thus preventing increased noise due to undersampling at F_{chop}.

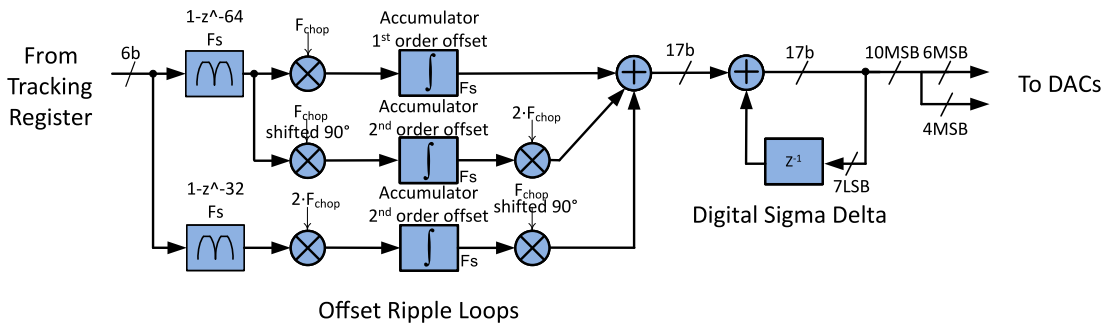


Fig. 4.6 Three independent digital offset ripple loops.

4.2.5 Digital Filters

To reject any remaining offset ripple owing to the limited resolution of the digital RRLs, a notch filter with transfer function $1+z^{-N}$, $N = F_s/F_{chop}/2$ is implemented in the main path. In ΣΔ ADCs, down-sampling is performed at this stage to reduce area and current consumption as the final update rate is usually much lower than F_s [20]. The approach can be applied here as well. However, if the intended application is rotational speed, then time domain jitter is a concern. The digital comparator translates the sampling frequency into jitter that is uniformly distributed between $\pm T_s$. For this case, the filters need to be operated at F_s, which would require N 6-bit registers. However, the notch design can be highly optimized for a tracking quantizer where successive samples only differ by ± 1. Only N 1-bit registers are needed to reconstruct the notch output at F_s, based on its initial condition.

4.3 Measurement Results

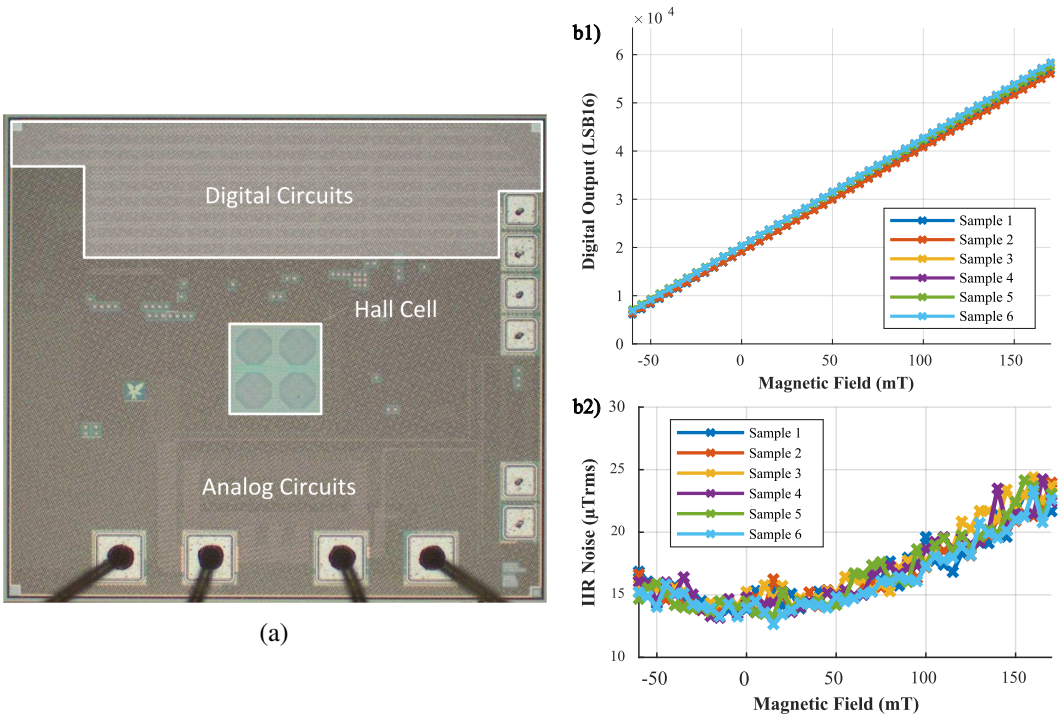
The tracking-based CT-ΣΔ-ADC magnetic sensor with digital offset ripple loops (D2D MS1) was fabricated in a 130 nm CMOS process. The chip micrograph is shown in Fig. 4.7a.

To validate the magnetic range, an electromagnet was used: measurements of 1000 IIR values via the digital interface were taken at points spaced 5 mT apart, and the resulting average values and standard deviations (Fig. 4.7b,c) were plotted as a function of the magnetic field. 230 mT range is proven, while 15 μTrms noise is achieved at 0 mT. This value increases at strong input fields, where the system's specifications are less stringent. The range asymmetry is due to an unipolar shift for the intended camshaft application.

For the residual offset results, the IC was inserted in a Zero Gauss Chamber. The proposed circuit techniques prove residual offsets of at most 16 μT at 25°C (Fig. 4.8a, 1σ and the maximum value measured precisely on 7 samples), starting from an initial offset of 4 mTrms.

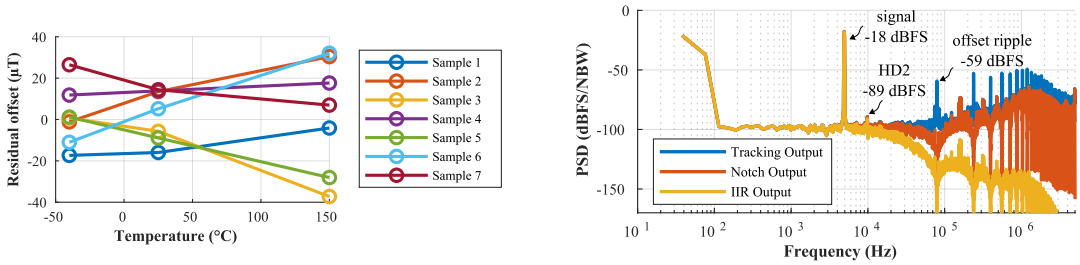
In a testmode, direct access to the comparator bitstream was available, enabling the offline reconstruction of the tracking ΣΔ register and notch and IIR filters, for the purpose of spectral analysis. A 30 mTpp and 5 kHz input magnetic signal was applied to the sensor IC. Estimates of the spectral densities of the main signals were performed for the plot in Fig. 4.8b. The second harmonic distortion of -71 dB is due to the lack of DC feedback around the analog integrator, but it is deemed sufficient for a measurement ADC. Due to the limited resolution of the offset feedback loops (10-bits), offset ripple is visible at F_{chop} but it is suppressed by the notch filter.

The relevant circuits occupy 0.25 mm^2 and consume 2.3 mA from the 2.4 V supply and 0.76 mA from the 1.5 V supply. Based on an established FOM [20], the system



(a) (b)

Fig. 4.7 (a) Micrograph of the switching sensor chip that includes the circuits described in this chapter. (b1) Digital output vs magnetic field. (b2) Measurement results of noise vs magnetic field.



(a) (b)

Fig. 4.8 (a) Measurement results of residual offset. (b) Frequency spectrum of tracking ΣΔ, notch and IIR outputs.

achieves 138 dB, a 3.1x improvement on state of the art (Table 6.1), with highlights on magnetic range and power consumption.

Chapter 5

Flash-based CT-ΣΔ-ADC magnetic sensor with digital-only demodulation (D2D MS2)

5.1 Introduction

In the previous chapter (Chapter 4) a CT ΣΔ ADC with tracking quantizer and digital offset ripple loops was proven [18]. However, the three digital offset ripple loops are fairly complex, and the system still needs a notch filter in the main path to suppress the remaining modulated offset caused by the limited resolution of the ripple loops. A system optimization is possible if the offset is passed through the ADC and then removed only by the notch filter. This can only be done if the tracking quantizer is replaced by a flash implementation, which is the subject of this chapter.

Furthermore, in that design, the analog demodulation chopper was placed above the integrating caps; together with the OTA output parasitic capacitors it resulted in a switched capacitor resistor with unintended effects, such as DC gain degradation and quantization noise folding. Implementing a CT ΣΔ with flash quantizer opens the path towards avoiding any analog "unchopper" and performing digital-only demodulation, which has the advantage of limiting the residual offset to that of the sensor and its switchbox. This system, referred to as D2D MS2 (Direct-to-Digital Magnetic Sensor 2), was proposed in our previous works [21, 22].

The principle of the D2D MS2 system, together with idealized time and frequency domain waveforms, is shown in Figure 5.1. An analog modulating chopper decouples the sensor signal from the ADC offset and its 1/f noise. The signal appears modulated at F_{chop} and its odd multiples. At the output of the ΣΔ converter, we find its slow-varying offset and its wide band noise added on top of those of the signal. The shaped quantization noise is shifted outside the useful bandwidth and, ideally, beyond the meaningful signal harmonics. A digital sinusoidal demodulator [23] then down converts

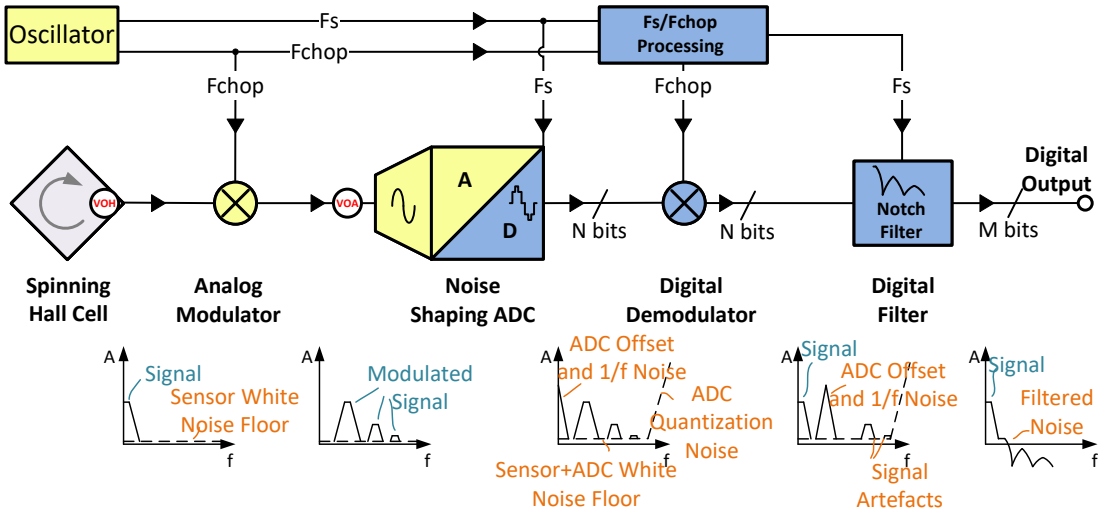


Fig. 5.1 System overview with highlight of the main signals and their frequency-domain representation.

the signal, while the offset and 1/f noise are shifted to higher frequencies and rejected by a simple notch filter. The multiplication with the sine wave results in an intermodulation sum (or signal artefact) at $2 \cdot F_{chop}$, but this too is suppressed by the notch functionality.

5.2 Circuit Implementation

The circuit implementation of the main component blocks of the D2D MS2 is described in the following subsections.

5.2.1 Spinning Current Hall Sensor

The spinning current Hall sensor consists of 2 Hall plates orthogonally coupled which consume 400 μA. The system is intended to work completely from a 1.5 V supply. The respective noise spectral density is 6.3 nV/$\sqrt{\text{Hz}}$. A 4-phase spinning scheme is employed to be able to reject also 2nd order effects, similar to Fig. 4.2. Different from Chapter 4, a 0°/90°/180°/270°rotation is used since the terminal shorting at the 90°rotation is so effective.

5.2.2 ADC Implementation

The block diagram of the circuit is shown in Figure 5.2. The first integrator consists of a a resistor-degenerated Gm-stage whose output current is integrated by a capacitor. A second integrator follows, and its output is sampled at F_s = 20 MHz and quantized by 7 comparators. Their 7-line thermometer output drives two 3-bit current steering DACs that implement the modulator's feedback paths.

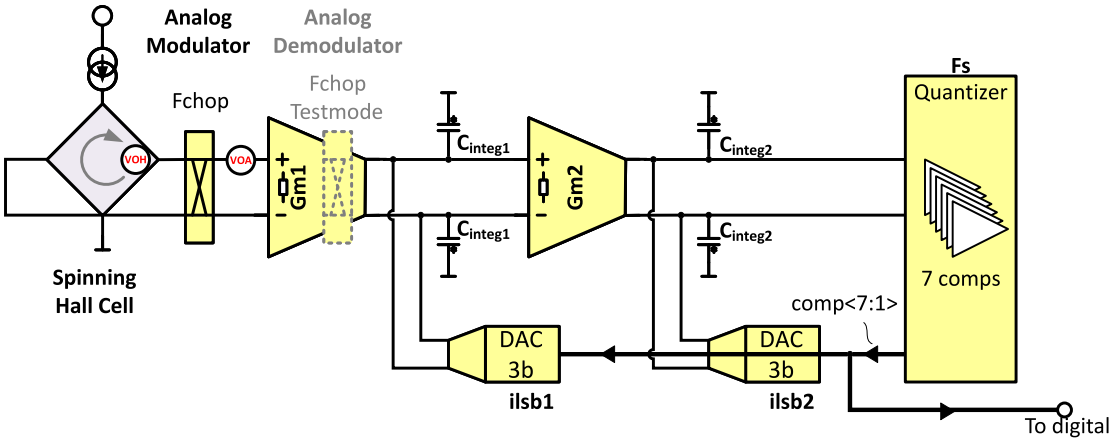


Fig. 5.2 Block diagram of the ADC.

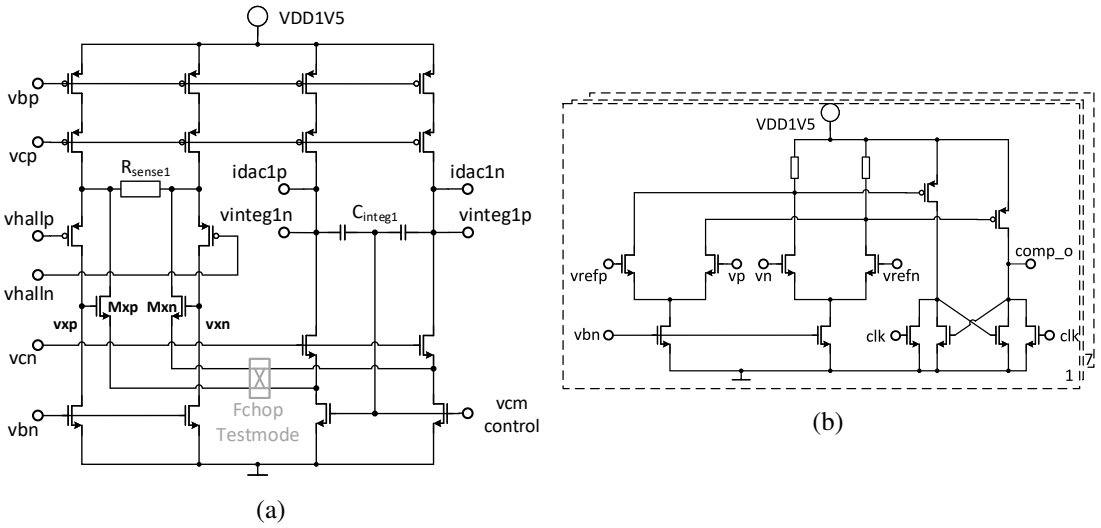


Fig. 5.3 Simplified schematic of a) the 1st integrator b) the comparator.

The first integrator, shown in Figure 5.3a, consumes 660 μA and achieves a voltage spectral density of 4.8 nV/$\sqrt{\text{Hz}}$, as determined by the input transistors and the 400 Ω sense resistor. Its initial offset is in the order of 440 $\mu V(1\sigma)$. A DC feedback loop ensures that the input voltage is copied across the sense resistor. The loop consists of a common drain and a common source stage. The compensation capacitor is not shown for simplicity. The folded cascode output current is integrated onto 4.7 pF output capacitors. A chopper, which can be activated in test mode, is placed at the G_m-stage output. The common mode feedback loop is not shown for simplicity.

The second integrator has relaxed requirements since it follows a gain stage. It consumes 160 μA and, with a lower G_{m2} of 31.25 μS, does not require local DC feedback. To ensure stability of the 2nd-order loop, the feedback through the first integrator must be 1.5 times weaker than the feedback through the second integrator. This is achieved by:

$$\frac{2 \cdot i_{lsbdac1} \cdot T_s}{R_{sense2} \cdot C_{integ1}} = \frac{i_{lsbdac2}}{1.5} \tag{5.1}$$

with $i_{lsbdac1} = 2 \cdot i_{lsbdac2} = 4\mu A$.

The gain of the second integrator is critical in a multi-bit implementation. Extensive behavioral simulations revealed an optimal gain of 0.66. This is achieved by setting C_{integ2} to 1.88 pF, in conjunction with the previously mentioned component values. The circuit sizing also reflects the scaling performed at each integrator level to optimize their output swings. This ensures they are operated in a linear range, while also relaxing the offset requirements on the quantizer. The double differential comparator (Fig. 5.3b) consumes 40 μA from the 1.5 V supply line. Each of the 7 instances uses a reference voltage taken from a resistor tap with a 160 mV step.

The 7-line output can be viewed as an element of the set {-7, -5, ..., 5, 7}, effectively controlling a feedback that spans a range of $\pm 7 \cdot V_{ref}$, with a step of $2 \cdot V_{ref}$, with input referred V_{ref} equal to $v_{ref} = i_{lsbdac1} \cdot R_{sense1}/2$. The current steering DAC was optimized to achieve good matching accuracy, as dynamic element matching techniques (such as bit rotation or data weighted averaging) were not employed in this design iteration. By using a drain saturation voltage of more than 400 mV and in combination with long transistors, a matching accuracy better than 0.5 %rms was achieved.

5.2.3 Digital Demodulation Techniques

In the analog demodulation case, the signal, as seen by the loop filter, remains in baseband, while offset and quantization noise are shifted to high frequency where they can be filtered by the digital filters. However, any block after the analog demodulating chopper contributes to the residual offset. In contrast, digital demodulation includes the full ADC in the offset rejection scheme, limiting residual offset to the contribution of the sensor and its switch box. However, signal harmonics appear at frequencies where quantization noise is substantial. Simple rectangular demodulation would significantly increase baseband noise due to quantization noise folding.

Conversely, a sinusoidal demodulation mechanism may be employed [21, 22]. The convolution of the noise around F_{chop} with demodulation sinusoidal tones will degrade the SNR by a few dB depending on the distance of F_{chop} from the quantization noise corner. A 7-bit sinusoidal signal is used for demodulation as shown in Figure 5.4a. It is compared in the same picture with a rectangular demodulation signal. For sake of comparison, in this case, they are all normalized to an amplitude of 64 LSB7.

5.2.4 Digital Filters

The digital filters implement the following transfer function:

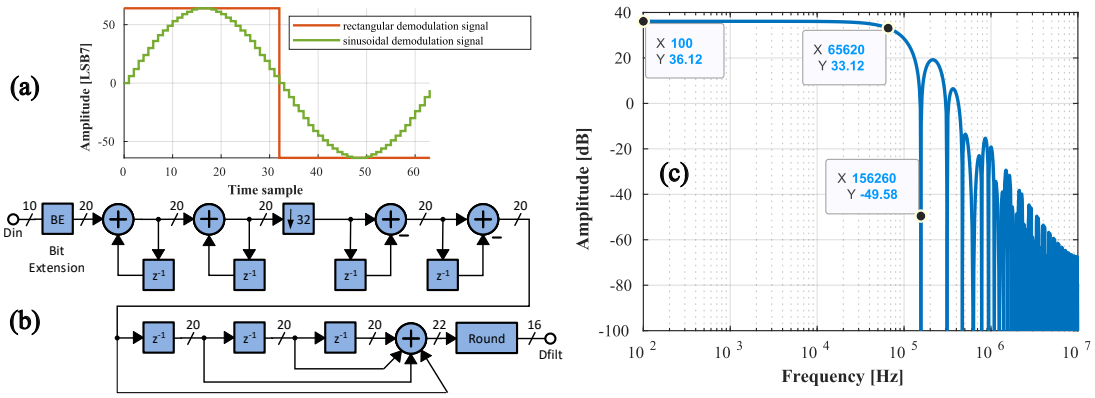


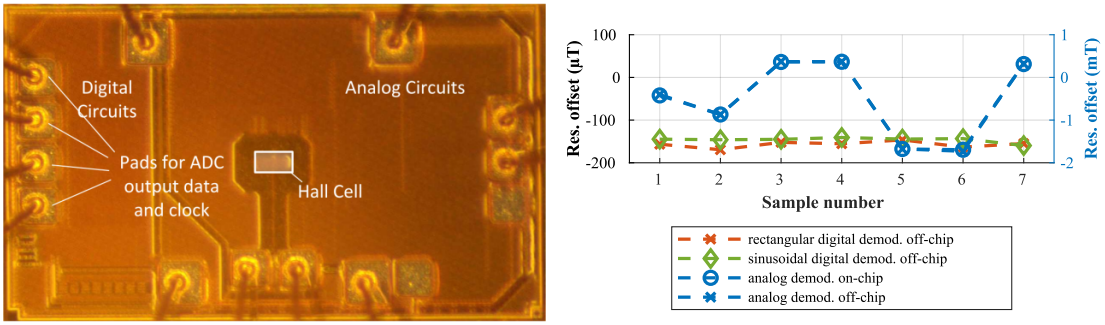
Fig. 5.4 a) The quantized sinusoidal demodulating signal compared to the rectangular one. b) Block diagram and c) transfer function of the digital filter.

$$H_{TF}(z) = \left(\frac{1-z^{-128}}{1-z^{-1}}\right) \cdot \left(\frac{1-z^{-32}}{1-z^{-1}}\right)^2 \tag{5.2}$$

In the right-hand part, the first parenthesis sets the final bandwidth to about 65 kHz and suppresses the offset content by creating notches at $F_{chop}/2$ and its harmonics, while the second-order part contributes to achieving a total slope of -60 dB/decade that effectively removes the quantization noise of the ΣΔ ADC and the intermodulation sum caused by sinusoidal demodulation. Notice that notches are required also at $F_{chop}/2$, because the 2nd order offset of the Hall sensor modulate at this frequency. Unlike a tracking quantizer implementation, the successive samples in a flash quantizer are not correlated which means that area optimization in the notch filter, is not possible. The amount of area depends on the required output rate.

The input to the filters is a 10-bit signal, created by multiplying a 6-bit sinusoidal waveform with the 4-bit output produced by the ΣΔ converter. $\left(\frac{1-z^{-32}}{1-z^{-1}}\right)^2$ can be realized as a 2nd order CIC with a decimation factor of 32, producing a 20-bit output. For an update rate of 625 kSa/s, this is followed by the implementation of $\frac{1-z^{-4}}{1-z^{-1}}$ at $F_s/32$, which consists of 4 20-bit registers and the corresponding adders.

The block diagram of the filter and its frequency response are shown in Fig. 5.4b,c. A bit or sign extension adds 10 bits for a 20-bit width. A typical CIC implementation follows, with the integrator run at 20 MHz and the derivators at 625kHz after the decimator stage. The final filter is a 4-sample moving average, with the result stored in a 22-bit register. Additional bits beyond the desired 16-bit resolution are discarded at the end. The estimated number of gates is 2560, which includes generating the sinus samples, a multiplier and the described filter. For a 130 nm technology, the area of a dual-input CMOS gate is in the order of 5 μm^2 for a total of 13000 μm^2. The situation becomes more favorable for smaller technology nodes. The digital blocks draw approximately 80 μA from the 1.5 V power supply.



(a) (b)

Fig. 5.5 (a) Micrograph of the testchip described in this chapter. (b) Residual offset for analog (right axis) and digital demodulation (left axis).

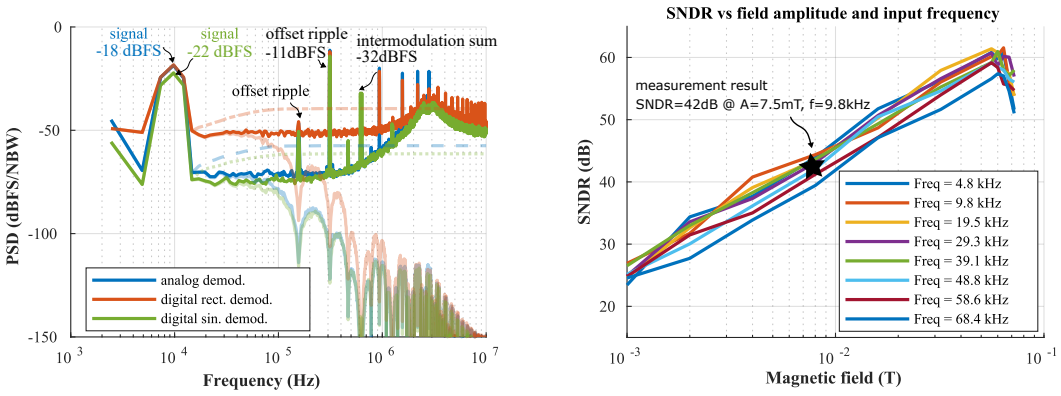
5.3 Measurement Results

The flash-based CT-ΣΔ-ADC magnetic sensor with digital-only demodulation (D2D MS2) was fabricated in a 130 nm CMOS process. The chip micrograph is shown in Figure 5.5a. The testchip contains the Hall sensor, the ADC and a digital part, plus the related infrastructure: bandgap and bias circuits, oscillator, regulator etc.

The digital part implements the rectangular digital demodulation and the CIC filters. It also makes available the internal registers via a 2-wire communication protocol. Finally, the circuits can be arranged in certain testmode configurations. For example, the digital demodulation may be disabled and the analog demodulating chopper enabled to compare the differences between the 2 options. The ADC data stream can be accessed at 3 output pads, together with the system clock. This is in order to enable spectral analysis, as well as offline testing in Matlab of different filters and demodulator options, such as sinusoidal demodulation.

Fig. 5.5b shows a residual offset of 920 μT (1σ) in the analog demodulation test mode, measured across 7 chips, starting from an initial offset in the range of 10 mTrms. The improvement of a factor of 10 is reasonable, but far from state of the art. This is due to the fact that only a portion of the readout circuit was chopped. Simulations show that including the current mirrors, cascodes and the DAC into the offset rejection scheme by moving the "unchopper" across the integrating capacitors, reduces the residual offset by ∼50x to 20 μT (1σ), but this may increase noise folding [18].

The residual offset with analog “unchopping” is plotted in Fig. 5.5b (blue lines) for both on-chip implementation and off-chip processing to demonstrate the reliability of the latter. It is compared to the digital demodulation techniques (red and green). Notice the different axes: right axis for analog demodulation and left axis for digital demodulation. There is a systematic contribution of -160 μT, most likely due to an asymmetry in the sensor environment: the spinning cell is composed of 2 Hall plates, instead of the typical quadruple configuration. However, the standard deviation of the set is 11 μT (1σ), which is comparable to state of the art.



(a) (b)

Fig. 5.6 (a)Averaged output spectra with analog and digital demodulation. The full-color lines represent the demodulated ΣΔ outputs, while the shadowed lines show their filtered counterparts. The shadowed dashed lines indicate the respective cumulative integrated noise. (b) Transient noise simulation results showing SNDR vs magnetic field amplitude and input frequency. Initial offset was set to 30 mT. Measurement result is shown for comparison.

Averaged ΣΔ output spectra based on the ADC data stream and for different configurations were generated for noise analysis. Due to a testmode limitation, the plots are based on 8192 points, making the frequency bin equal to about 2.44 kHz. Several sections can be averaged together to get a smoothing function.

For Fig. 5.6a, an A = 7 mT and Fin = 9.8 kHz magnetic signal was applied to the sensor IC. In the analog demodulation case, the signal is at -18 dBFS. No distortions are visible in the plot. The offset ripple at F_{chop} = 312 kHz represents the combined contributions of the 1st order Hall offset and the readout stage offset. At $F_{chop}/2$, a smaller offset ripple is visible: 2nd order offsets from the Hall sensor reside there. The CIC filter is set to have the notches at $F_{chop}/2$ and its multiples, thus suppressing both effects. The +40 dB/decade shaping of the quantization noise is also visible but attenuated by the filters (shadowed lines). The system is limited by white noise, as indicated by power spectral density integration (shadowed dashed lines).

To achieve low residual offset, digital demodulation is preferred, thus including all readout circuit in the chopping scheme. The analog demodulation chopper is disabled via a testmode command. The signal now appears at F_{chop} ±9.7 kHz, in the vicinity of the quantization noise corner. The readout stage and the 1st order Hall offsets remain at DC. The secondary offsets are modulated at $F_{chop}/2$. The digital demodulator sends the offset components at $F_{chop}/2$ and F_{chop} and returns the signal to baseband. A rectangular demodulator folds back significant quantization noise from the odd multiples of F_{chop}, as seen in Figure 5.6a, orange graph. The noise penalty is an astonishing 11x or about 10 dB.

However, in the case of sinusoidal demodulation, performed offline, the gain is reduced by a factor of $\pi/2$ (4 dB), but the noise level is simultaneously decreased by a factor of 1.2. This results in an SNR degradation of 2.3 dB. This deviates from the

expected theoretical 1 dB, since the noise around the modulated signal is not purely white but contains significant quantization noise. While the typical sensitivity is in the vicinity of 240 LSB16/mT, in the sinusoidal demodulation case, this is scaled to 152 LSB16/mT, with a noise level (averaged across the 7 measured chips) of 10 LSB16. This can be calculated to 66 μTrms in the 65 kHz bandwidth.

Transient noise simulations were performed to demonstrate the magnetic range. The initial offset was set to 30 mT, corresponding to a 3σ value. The magnetic field amplitude and input frequency were swept to generate the SNDR plots in Figure 5.6b. The results show that a magnetic range of $\pm$60 mT is achievable before noise degradation exceeds 15%, with a peak SNR of 58.4 dB. The dynamic measurement at A = 7.5 mT and Fin = 9.8 kHz is in good agreement with the simulation results. The SNDR of the standalone ΣΔ ADC is 4.4 dB higher, since the sensor noise dominates the system noise, exceeding the readout stage noise by a factor of 1.32.

The area occupied by D2D MS2 is 0.11 mm^2. The power consumption can be calculated to 2.55 mW, as the relevant blocks draw 1.7 mA from the 1.5 V supply voltage.

Table 6.1 shows a comparison of D2D MS2 to other CMOS Hall sensors. The architecture achieves a FOM_{DR} of 130 dB, comparable to the best recent state-of-the-art CMOS Hall sensors, while featuring a low supply voltage of 1.5 V, the smallest area and at least 2.6x improvement in power consumption. A comprehensive overview of the table will be provided in Chapter 6.

Chapter 6

Performances of the Proposed Magnetic Sensors

The novel techniques introduced in the previous chapters created the context for improved magnetic range at the same time with reduced power consumption and area. This is visible in Table 6.1, which compares the two proposed prototypes (D2D MS1 and D2D MS2) with state-of-the-art CMOS magnetic sensors. Except for [5] they are the only entries with a direct-to-digital readout circuit (*D2D*). However, many of the analog interface sensors in the table (*A*) have a digital output, i.e., they have an on-chip ADC at the end of the chain, which enforces the idea that direct-to-digital interfaces are optimal if well designed.

With reference to Table 6.1, the tracking-based CT-ΣΔ-ADC magnetic sensor of Chapter 4 (D2D MS1) is implemented in 130 nm CMOS. To benefit from more sensitivity, a higher 2.4 supply was used for the Hallbias. The digital part, however, and part of the analog blocks are supplied at 1.5 V. In terms of area, 0.25 mm^2 is the lowest footprint except for [26] and D2D MS2. The residual offset comes behind [5], [25] and D2D MS2. The magnetic range is the highest reported, with at least a factor of 1.7x improvement. The dynamic range is second behind [25]. The power consumption of the system is the lowest behind D2D MS2, benefiting from the low supply voltage and current consumption. The reported noise, power consumption, and area values include the contributions from the digital blocks, as this is a digital output magnetic sensor. The bandwidth of the system is the primary limitation, having been constrained by noise requirements. Consequently, the achieved bandwidth is significantly lower than the typical requirements for current sensors, which often operate in the hundreds of kHz range [17]. When considering all the stated results in the Schreier FOM_{DR}, D2D MS1 achieves 138 dB, a 3.1x improvement on state of the art.

The flash-based CT-ΣΔ-ADC magnetic sensor of Chapter 5 (D2D MS2) is the only 1.5 V implementation in Table 6.1, an important trend for modern sensors. There are other highlights of the proposed design. It shows by far the smallest area. With 2.55 mW, it results in at least 2.6x improvement in power consumption. The 11 $\mu T(1\sigma)$ residual

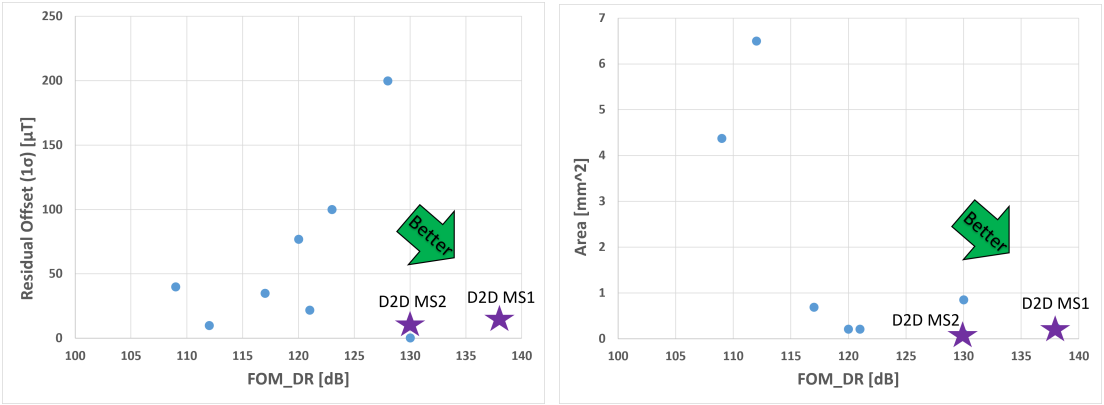
Table 6.1 Performance summary and comparison with state-of-the-art CMOS magnetic sensors.

	This Work		[10]	[5]	[11]	[17]	[12]	[24]	[25]
	D2D MS1	D2D MS2	'05	'12	'17	'17	'22	'22	'25
Technology [nm]	130	130	600	350	180	180	180	130	180
Supply [V]	2.4/1.5	**1.5**	3	3.3	3.3	5	3.3	3	1.8
Area [mm^2]	0.25	**0.11**	4.9[a]	6.5[a]	0.69[b]	4.38	0.21	1.12[a]	0.85
Offset [μT]	16 (σ)	**11** (σ)	<200	10 (σ)	<35	<40	22 (σ)	<100	0.3 (σ)
Noise [μTrms]	15	66	24	4	9	136	47	65	0.3
Noise Density [$\mu T/\sqrt{Hz}$]	0.13	0.26	0.14	0.13	0.34	0.22	0.05	0.33	0.06
Range [mT]	**230**	120	130	30	70	25	21	200	50
DR [dB]	**75**	56	66	68	69	36	44	61	95
Bandwidth [kHz]	14	65	30	1	0.72	400	820	40	0.03
Power [mW]	6.8	**2.55**	17.1[a]	41.3[a]	9.9[a]	20.0	16.8	21.9[a]	9.5
FOM_{DR} [dB][c]	**138**	130	128	112	117	109	121	123	130
FOM_{off} [dB][d]	137	**146**	110	104	106	120	128	120	129
Digital Output	Yes	Yes	No	Yes	Yes	No	Yes	No	Yes
Readout Circuit	D2D	D2D	A	D2D	A	A	A	A	A

[a] total chip area/current consumption as no highlight of relevant circuits is given
[b] estimated from micrograph figure [c] $FOM_{DR} = 10 \cdot \log10[(P_{sig}/\sigma_n^2) \cdot F_{BW}/Power]$
[d] $FOM_{off} = 10 \cdot \log10[(P_{sig}/\sigma_{os}^2) \cdot F_{BW}/Power]$

offset is similar to [5] and behind only [25]. The ±60 mT magnetic range is the second best after D2D MS1. It can be improved by increasing the sense resistor of the readout stage, with a small noise penalty. The 65 kHz bandwidth is moderate, falling within the mid-range of the values listed in the table. The noise and noise density (noise divided by bandwidth) performance are not outstanding, due to reduced sensitivity resulting from the lower supply voltage. Despite the associated decrease in sensitivity, the system still achieves a FOM_{DR} of 130 dB, which is better or equal to most state of the art, except for D2D MS1. When considering offset as the limiting factor in the system's ability to measure or detect magnetic fields, the architecture achieves a FOM_{off} of 146 dB, a 2.8x improvement on D2D MS1 and surpassing the rest of the state-of-the-art solutions by more than 7x.

Since FOM_{DR} does not contain the residual offset nor area in its formula, it is interesting to see how the prototypes described in Chapters 4 and 5 compare to other CMOS Hall sensors in terms of FOM_{DR} vs residual offset and FOM_{DR} vs area. This is shown in Figure 6.1. The ideal direction is towards the lower right corner of the graph, where better performance is achieved. Although D2D MS1 is best in terms of FOM_{DR}, D2D MS2 shows better residual offset and area, but at the cost of a lower FOM. However, as will be explored in the final section, this development paves the way for higher bandwidths, a key parameter for next-generation of magnetic sensors in current sensing applications.



(a) (b)

Fig. 6.1 How the prototypes presented in this thesis compare to other CMOS Hall sensors in terms of (a) FOM_{DR} vs residual offset and (b) FOM_{DR} vs area.

Chapter 7

Conclusions

7.1 Summary

This thesis presented two monolithic integrated direct-to-digital readout architectures for Hall sensors (D2D MS1 and D2D MS2), realized in a 130 nm technology. By removing the preamplifier and the analog offset ripple loops in the traditional analog interfaces, wider magnetic ranges and power efficiency were obtained at the same time. The ADC was connected directly to the spinning-current Hall cell by means of Gm-C techniques to avoid interfering with the sensor. By making use of the inherent anti-aliasing function of the feedback compensated continuous-time sigma-delta (CT $\Sigma\Delta$) ADCs, notch filters were effectively implemented in the digital domain at the oversampling frequency to suppress offset without compromising performance. The analog real estate was reduced and complexity was shifted to the digital domain, thus providing scalable solutions towards more advanced technology nodes and lower supply voltages.

Chapter 1 introduced the field of the doctoral thesis: automotive, industrial, consumer and IoT applications are complex systems that require sensor solutions to monitor parameters, process them and respond to the environment. Within the overall sensor market, magnetic sensors were described as playing a key role in enabling precise control of advanced systems in both the traditional automotive market, but also in the fast booming consumer end-market. Several magnetic sensing technologies were reviewed, including the promising TMR effect with its high sensitivity, but the Hall sensors continue to be a crucial element due to CMOS compatibility, high offset-related accuracy, good linearity even at very high fields, and lack of hysteretic effects. An area for improvement was identified, focusing on enhancing the magnetic range, expanding digital functionality, lowering the supply voltage and reducing costs, all while at least preserving the existing performance levels in terms of offset and noise.

Chapter 2 provided an introduction to the Hall device, aiming to familiarize the reader with its characteristics and challenges, thereby laying the groundwork for a deeper understanding of the circuit techniques presented in subsequent chapters. The Hall

effect was explained, along with the process-dependent variations in sensitivity and resistance that can impact sensor performance, followed by an overview of selected bias circuits that ensure technological, temperature, and stress stability. Additionally, offset compensation techniques were discussed, with a focus on the spinning-current technique, a dynamic approach that differentiates between the sensor signal and offset, enabling subsequent filtering and offset reduction.

Chapter 3 introduced the world of signal processing paths and readout circuits, covering high-accuracy techniques such as chopping, and providing an in-depth examination of the fundamental blocks that make up these systems. A comprehensive literature review was then conducted, encompassing traditional analog sensor interfaces and a few direct-to-digital sensor interfaces, which aim to connect the ADC directly to the sensor. This review revealed opportunities for improvement in terms of area, power consumption and dynamic range, laying the groundwork for the subsequent chapters.

A first system (D2D MS1) was proposed in Chapter 4 and realized as a 1st order CT ΣΔ loop with a tracking quantizer based on a 1-bit analog comparator. This was combined with three digital offset ripple loops and a special timing sequence to achieve 16 μT (1σ) offset and 15 μTrms noise in a magnetic range of 230 mT, yielding a FOM_{DR} of 138 dB, at least 3.1x better than state of the art. The chapter began by providing context for the intended application of the sensor IC. A systematic development of the system was then presented, using Simulink for step-by-step modeling, accompanied by simulation results. Next, the transistor-level implementation was described in detail, including simplified block diagrams of each component block. The chapter concluded with a discussion of the measurement results, including graphs of key performance metrics such as magnetic range, sensitivity, initial and residual offset, noise and jitter.

A second system (D2D MS2) was proposed in Chapter 5 aiming to further improve power consumption and area, while also paving the way for increased bandwidth. The CT ΣΔ ADC was implemented with a flash-based inner quantizer. This allowed the upmodulated signal to be converted and thus enabled digital-only demodulation, limiting the residual offset to that of the sensor and its switchbox and bypassing the need of digital offset ripple loops. By using a sinusoidal signal for demodulation, 11 μT (1σ) offset was obtained without compromising on noise level and with a small footprint of 0.11 mm^2. Together with a power consumption of 2.6 mW and a magnetic range of 120 mT, the architecture achieved an offset related FOM of 146 dB, outperforming the first system by a factor of 2.8, while surpassing other state-of-the-art CMOS Hall sensors by more than 7 times. Following a similar structure to the previous chapter, the system development was initially outlined, with Simulink used to create a step-by-step model and with simulation results validating the design. This was followed by a detailed description of each system block, which included simplified diagrams that illustrated the transistor-level implementation. Finally, measurement results were discussed, including

initial and residual offset, spectral analysis of the ΣΔ output and SNDR vs input signal amplitude and frequency.

To summarize the key principles presented in the thesis, Chapter 6 began by contrasting traditional analog sensor interfaces with the two proposed direct-to-digital implementations, illustrating the expanded role of digital blocks in the direct-to-digital designs. The comparison of the two prototypes against other CMOS Hall sensors was then presented in a comprehensive table, which summarized key performance metrics such as area, offset, magnetic range, and power consumption. This comparison was further visualized through graphs of FOM_{DR} versus area and FOM_{DR} versus residual offset, providing a detailed overview of how the two prototypes stacked up against state-of-the-art CMOS Hall sensors.

Finally, this chapter presents a summary of the thesis, highlighting the original contributions and listing the original publications. The thesis concludes with perspectives for further developments.

7.2 Original Contributions

1. Conducted an extensive review of the existing literature on Hall sensors and analog readout circuits [6, 9].

2. Realized D2D MS1 – the tracking-based CT-ΣΔ-ADC magnetic sensor with digital offset ripple loops [2, 9].

   (a) Demonstrated the feasibility of a ΣΔ system without decimation, enabling low-jitter switching sensors with ΣΔ ADCs [2].

   (b) Created and simulated the Matlab&Simulink model for proof of concept [2].

   (c) Implemented and simulated the transistor level design of each component block of D2D MS1 [2].

   (d) Designed a novel timing sequence for Hall sensors [2, 8].

   (e) Introduced the concept of reusing the ΣΔ DAC as offset ripple DAC [2].

   (f) Introduced a noise-shaped ΣΔ DAC to avoid propagating truncation errors from the (limited resolution) offset ripple DAC [2].

   (g) Created an accurate voltage-to-current conversion method using ΣΔ feedback in a resistive degenerated readout stage [2].

   (h) Improved the orthogonal digital based triple ripple reduction loop to avoid underaliasing effects [2].

   (i) Created a Verilog-A model of the digital part of D2D MS1 to allow fast and accurate simulations of the analog components [2].

   (j) Performed post-processing on the measurement data of the silicon samples from D2D MS1 [2].

3. Invented and realized D2D MS2 – the flash based CT-ΣΔ-ADC magnetic sensor with digital-only demodulation [1, 3, 7, 9].

   (a) Created and simulated the Matlab&Simulink model for proof of concept [3].

   (b) Implemented and simulated the transistor level design of each component block of D2D MS2 [1].

   (c) Investigated the limitations and drawbacks of digital demodulation techniques [1, 3]

   (d) Introduced digital-only demodulation and sinusoidal demodulation techniques [1, 3, 5, 7].

   (e) Performed measurements and post-processing on the measurement data of the silicon samples from D2D MS2 [1].

4. Introduced the ping-pong technique in a hysteresis comparator for a magnetic sensor [4].

7.3 List of Original Publications

Journal Papers

1. **D. -I. -D. Stoica**, A. Ciobanașu, A. Gheorghe, M. Motz and G. Brezeanu, “A Direct-to-Digital Readout Architecture for CMOS Hall Sensors,“ in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 72, no. 11, pp. 1655-1659, Nov. 2025, doi: 10.1109/TCSII.2025.3605969, ISI, WOS: 001610854500035 (Q1, 2025)

Conference Papers

2. **D. -I. -D. Stoica**, M. Motz, A. Gheorghe, I. -I. Cristea and L. Turică, "A 75 dB DR, 0.13 uT/Hz Hall Sensor with CT-SD-ADC, Digital Chopper Ripple Rejection Loops and Custom Nano-Timing Techniques," 2024 IEEE European Solid-State Electronics Research Conference (ESSERC), Bruges, Belgium, 2024, pp. 524-527, doi: 10.1109/ESSERC62670.2024.10719446, ISI, WOS: 001349548800132.

3. **D. -I. -D. Stoica**, I. -A. Nica, A. Ciobanaşu and G. Brezeanu, "A Continuous-Time Sigma-Delta ADC for Chopped Sensors with Digital Only Demodulation," 2024 International Semiconductor Conference (CAS), Sinaia, Romania, 2024, pp. 1-4, doi: 10.1109/CAS62834.2024.10736855, ISI, WOS: 001361909500036.

4. A. Obuhov, **D. -I. -D. Stoica**, I. -A. Nica and A. Cracan, "A Low Offset Ping-Pong Hysteresis Comparator for Magnetic Sensors," 2024 International Semiconductor Conference (CAS), Sinaia, Romania, 2024, pp. 241-244, doi: 10.1109/CAS62834.2024.10736722, ISI, WOS: 001361909500051.

5. A. Ciobanașu, **D. -I. -D. Stoica**, I. -I. Cristea, A. Cracan, R. Bozomitu, "A Digital Demodulation-Based Architecture for Offset-Free Chopped Sensor Signal Paths Using Oscillator-Based ADCs," 2025 International Semiconductor Conference (CAS), Sinaia, Romania, 2025, pp. 239-242, doi: 10.1109/CAS66707.2025.11222247

6. **D. Stoica** and M. Motz, "A dual vertical Hall latch with direction detection," 2013 Proceedings of the ESSCIRC (ESSCIRC), Bucharest, Romania, 2013, pp. 213-216, doi: 10.1109/ESSCIRC.2013.6649110, IEEE: 6649110.

Patents

7. **Dan Ioan Dumitru Stoica** and Ioan-Alexandru Nica, "Sensor circuit," US 2025/0062774 A1, Feb. 20, 2025

8. Andrei-Sorin Gheorghe, **Dan Ioan Dumitru Stoica**, Ilie-Ionut Cristea, "Sigma-delta analog to digital converter and method for converting an analog input signal to a digital output signal at a sampling frequency," US 2024/0250693 A1, Jul. 25, 2024

Workshops

9. **Dan Stoica**, "Direct-to-Digital Interfaces for CMOS Hall-Effect Sensors," presented in *The Fourth Sensor Interfaces Meeting (IEEE SIM'25)*, Veldhoven, The Netherlands

Regarding the list of publications, paper number 6 was published before the doctoral program, but it has relevance to the thesis subject as the author experiment of analog interface sensors. Additionally, presentation number 9 was a keynote speech and, as such, was not published.

7.4 Perspectives for Further Developments

In terms of enabling lower supply voltages for Hall sensors, the oscillator-based ADCs offer a promising solution, due to their core component – the voltage controlled oscillator (VCO) – which can operate effectively at very low power supply. A design demonstrating this capability [27] achieved a supply voltage of 1 V utilizing a digital-only demodulation technique, as discussed in Chapter 5. This approach eliminates the need for analog

offset ripple loops and avoids the intermodulation mix between the chopping and the oversampling frequencies into baseband.

In another development, a digital multi-path sensor can be imagined (Fig. 7.1) to improve bandwidth, the primary limitation of the proposed systems. A Hall device is used for its low frequency performance, which can be achieved by the spinning-current technique. A flash-based CT-ΣΔ-ADC digitizes the information bringing the up-modulated signal and the offset in the digital domain. After sinusoidal digital demodulation, to reduce delay, the notch filters are avoided and a fully digital offset ripple loop is introduced to suppress offset. An IIR filter than sets the bandwidth to 2 kHz, an optimum obtained for hybrid sensors. In parallel, a coil is used in voltage mode and followed by another flash-based CT-ΣΔ-ADC. Its signal increases with frequency making it preferable for high frequency operation. A high-pass filter rejects the offset of the readout stage and an 2 kHz low pass filter, identical to the one from the low frequency path, plays the integration role that is mandatory in a coil signal path. The outputs of the two signal paths are summed together for a smooth 10 MHz bandwidth with virtually no gain errors (digital filters), with a very good offset related accuracy as set by the spinning Hall system and a very good SNR as given buy a hybrid Hall-coil system. Surely the quantization noise may be large in the 1-10 MHz band. This either may be enough for applications for which fast response is more important than repeatability or it can be reduced by adding more quantizer bits and/or increasing the sampling frequency.

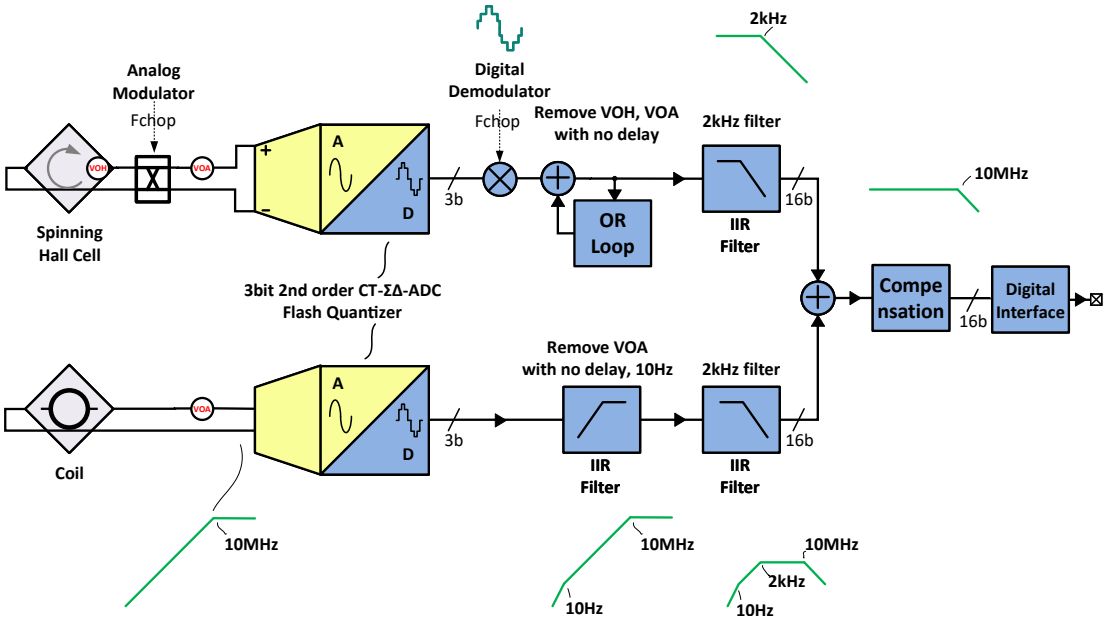


Fig. 7.1 Block diagram of a digital multi-path sensor combining direct-to-digital interfaces of a Hall plate and of a coil to achieve high SNR at the same time with high bandwidth.

References

[1] Magnetic sensors report 2024. https://www.yolegroup.com/product/report/magnetic-sensors-2024/. Accessed: 2025-08-19.

[2] Infineon magnetic sensors. https://www.infineon.com/products/sensor/magnetic-sensors. Accessed: 2025-08-25.

[3] P. Ripka and Michal Janosek. Advances in magnetic field sensors. *Sensors Journal, IEEE*, 10:1108 – 1116, 07 2010.

[4] Radivoje S. Popović. *Hall effect devices*. Series in sensors. Institute of Physics Pub, Bristol Philadelphia, second edition edition, 2004.

[5] Mario Motz, Udo Ausserlechner, Manfred Bresch, Uwe Fakesch, Bernhard Schaffer, Christian Reidl, Wolfgang Scherr, Gerhard Pircher, Michael Strasser, and Volker Strutz. A miniature digital current sensor with differential Hall probes using enhanced chopping techniques and mechanical stress compensation. In *2012 IEEE Sensors*, pages 1–4, Taipei, Taiwan, October 2012. IEEE.

[6] Josef Schweda. *Analysis of Shift Mechanisms in BiCMOS Hall Devices with Scope of a Precise SPICE Simulation Model*. PhD thesis, Technische Universität Wien, 2007.

[7] D. Draxelmayr and R. Borgschulze. A self-calibrating hall sensor ic with direction detection. *IEEE Journal of Solid-State Circuits*, 38(7):1207–1212, 2003.

[8] P.J.A. Munter. A low-offset spinning-current hall plate. *Sensors and Actuators A: Physical*, 22(1):743–746, 1990.

[9] A. Bilotti, G. Monreal, and R. Vig. Monolithic magnetic hall sensor using dynamic quadrature offset cancellation. *IEEE Journal of Solid-State Circuits*, 32(6):829–836, 1997.

[10] M. Motz, D. Draxelmayr, T. Werth, and B. Forster. A chopped hall sensor with small jitter and programmable "true power-on" function. *IEEE Journal of Solid-State Circuits*, 40(7):1533–1540, July 2005.

[11] Sebastien Leroy, Stefan Rigert, Arnaud Laville, Andrea Ajbl, and Gael F. Close. Integrated hall-based magnetic platform for position sensing. In *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, pages 360–363, 2017.

[12] Robbe Riem, Johan Raman, and Pieter Rombouts. A 2 ms/s full bandwidth hall system with low offset enabled by randomized spinning. *Sensors*, 22(16), 2022.

[13] M. Ortmanns and F. Gerfers. *Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations*. Springer Series in Advanced Microelectronics. Springer, 2006.

[14] C.C. Enz and G.C. Temes. Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization. *Proceedings of the IEEE*, 84(11):1584–1614, 1996.

[15] Yongjia Li, Mario Motz, and Leneesh Raghavan. A fast th overcurrent detector for a spinning hall current sensor with ping-pong and chopping techniques. *IEEE Journal of Solid-State Circuits*, 54(7):1852–1861, 2019.

[16] **Dan Stoica** and Mario Motz. A dual vertical Hall latch with direction detection. In *2013 Proceedings of the ESSCIRC (ESSCIRC)*, pages 213–216, Bucharest, Romania, September 2013. IEEE.

[17] Junfeng Jiang and Kofi A. A. Makinwa. Multipath wide-bandwidth cmos magnetic sensors. *IEEE Journal of Solid-State Circuits*, 52(1):198–209, 2017.

[18] **Dan-Ioan-Dumitru Stoica**, Mario Motz, Andrei Gheorghe, Ilie-Ionuţ Cristea, and Liviu Turică. A 75 db dr, 0.13 ut/hz hall sensor with ct-sd-adc, digital chopper ripple rejection loops and custom nano-timing techniques. In *2024 IEEE European Solid-State Electronics Research Conference (ESSERC)*, pages 524–527, 2024.

[19] Ilie-Ionut Cristea Andrei-Sorin Gheorghe, **Dan Ioan Dumitru Stoica**. Sigma-delta analog to digital converter and method for converting an analog input signal to a digital output signal at a sampling frequency, US 2024/0250693 A1, Jul. 25, 2024.

[20] Richard Schreier and Gabor C. Temes. *The FirstOrder Delta Sigma Modulator*, pages 21–62. 2005.

[21] **Dan-Ioan-Dumitru Stoica**, Ioan-Alexandru Nica, Andrei Ciobanaşu, and Gheorghe Brezeanu. A continuous-time sigma-delta adc for chopped sensors with digital only demodulation. In *2024 International Semiconductor Conference (CAS)*, pages 1–4, 2024.

[22] **Dan-Ioan-Dumitru Stoica**, Andrei Ciobanaşu, Andrei Gheorghe, Mario Motz, and Gheorghe Brezeanu. A direct-to-digital readout architecture for cmos hall sensors. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 72(11):1655–1659, 2025.

[23] **Dan Ioan Dumitru Stoica** and Ioan-Alexandru Nica. Sensor circuit, US 2025/0062774 A1, Feb. 20, 2025.

[24] Michaela Keil, Johannes Gert Janschitz, and Mario Motz. A hall effect magnetic sensor with ratiometric output, utilizing a self-regulating chopped amplifier for compensation of offset, temperature and lifetime drift effects. In *2022 Austrochip Workshop on Microelectronics (Austrochip)*, pages 1–4, 2022.

[25] Floris J. P. van Mourik, Sining Pan, Karen M. Dowling, and Kofi A. A. Makinwa. 27.2 a voltage-biased cmos hall sensor with $1.0\mu\mathrm{T}(3\sigma)$ offset and a $60\mathrm{nT}/\sqrt{\mathrm{hz}}$ noise-floor. In *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, volume 68, pages 1–3, 2025.

[26] Robbe Riem, Johan Raman, Jonas Borgmans, and Pieter Rombouts. A low-noise instrumentation amplifier with built-in anti-aliasing for hall sensors. *IEEE Sensors Journal*, 21(17):18932–18944, 2021.

[27] Andrei Ciobanaşu, **Dan-Ioan-Dumitru Stoica**, Ilie-Ionuț Cristea, Arcadie Cracan, and Radu-Gabriel Bozomitu. A digital demodulation-based architecture for offset-free chopped sensor signal paths using oscillator-based adcs. In *2025 International Semiconductor Conference (CAS)*, pages 239–242, 2025.